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TYPE SN75369 DUAL MOS DRIVER

BULLETIN NO. DL-S 7712380, APRIL 1976 - REVISED APRIL 1977

MOS MEMORY INTERFACE

- Dual Inverting MOS Driver
- Low Standby Power Dissipation
- Versatile Interface Circuit for Use between TTL Levels and Level-Shifted High-Current, High-Voltage Systems
- Inputs May Be Level-Shifted by Use of a Current Source or Capacitive Coupling or Driven Directly by a Voltage Source
- Designed to Be Functionally Interchangeable with National DS0026
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs and MOS Shift Registers
- V_{CC} Supply Voltage Variable over Wide Range to 22 Volts Maximum with Respect to V_{EE}
- Operates from Standard Bipolar and/or MOS Supply Voltage
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation

description

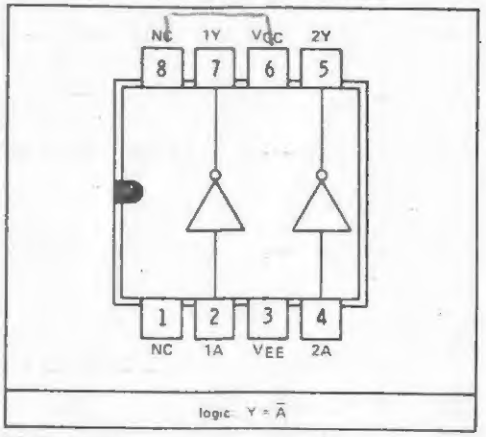
The SN75369 is a monolithic dual MOS driver and interface circuit that operates with either current-source or voltage-source input signals. The device accepts appropriate level-shifted input signals from TTL or other logic systems and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and/or timing inputs for several types of MOS RAMs and MOS shift registers.

The SN75369 operates from standard MOS and/or bipolar supplies in most applications. This device has been optimized for operation with V_{CC} supply voltage from 12 volts to 20 volts positive with respect to V_{EE}. However, it is designed so as to be usable over a wide range of V_{CC}.

Inputs of the SN75369 are referenced to the V_{EE} terminal and contain a series current-limiting resistor. The device will operate with either positive current input signals or voltage input signals that are positive with respect to V_{EE}. In many applications the V_{EE} terminal is connected to the MOS V_{DD} supply of −12 volts to −15 volts with the inputs to be driven from TTL levels or other positive voltage levels. The required negative-level shifting may be done with an external p-n-p transistor current source or by use of capacitive coupling and appropriate input voltage pulse characteristics.

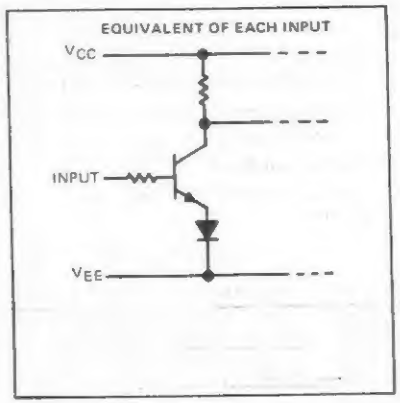
The SN75369 is characterized for operation from 0°C to 70°C.

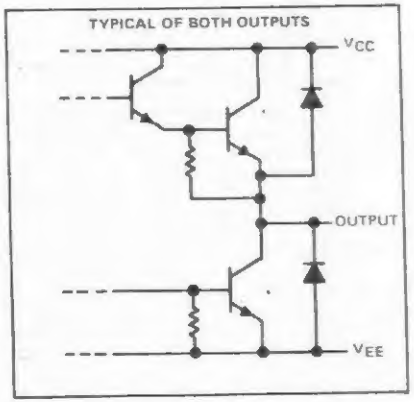
JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC = No internal connection

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC} (see Note 1) . . . . . −0.5 V to 22 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. Voltage values are with respect to the V_{EE} terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the JG package, SN75369 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	20	22	V
Operating free-air temperature, T_A	0		70	°C

definition of input logic levels

PARAMETER		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	2.5		4.5	V
V_{IL}	Low-level input voltage			0.5	V
I_{IH}	High-level input current	8		20	mA
I_{IL}	Low-level input current			27	mA

electrical characteristics over recommended ranges of V_{CC} and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS (See Note 3)		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −15 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.5 V,	I_{OH} = −50 μA	V_{CC}−1	V_{CC}−0.7		V
		I_{IL} = 0.7 mA,	I_{OH} = −50 μA				
		V_{IL} = 0.5 V,	I_{OH} = −10 mA	V_{CC}−2.3	V_{CC}−1.8		
		I_{IL} = 0.7 mA,	I_{OH} = −10 mA				
V_{OL}	Low-level output voltage	V_{IH} = 2.5 V,	I_{OL} = 10 mA		0.15	0.3	V
		I_{IH} = 8 mA,	I_{OL} = 10 mA				
		V_{CC} = 10 V to 22 V,	V_{IH} = 2.5 V, I_{OL} = 30 mA		0.2	0.4	
		V_{CC} = 10 V to 22 V,	I_{IH} = 8 mA, I_{OL} = 30 mA				
V_{OK}	Output clamp voltage	V_I = 0 V,	I_{OH} = 20 mA			V_{CC}+1.5	V
V_I	Input voltage	I_I = 20 mA			3.7	5	V
		I_I = 8 mA			2.4	3	
		I_I = 0.7 mA			0.4	0.6	
I_I	Input current	V_I = 4.5 V			27	45	mA
		V_I = 2.5 V			9	15	
		V_I = 0.5 V				1.5	
$I_{CC(H)}$	Supply current from V_{CC}, both outputs high	V_{CC} = 22 V, Both inputs at 0 V,	No load			0.5	mA
$I_{CC(L)}$	Supply current from V_{CC}, both outputs low	V_{CC} = 22 V, Both inputs at 3 V,	No load		7	12	mA

†All typical values are at V_{CC} = 20 V and T_A = 25°C.
NOTE 3: Many of these parameters are specified independently for either voltage source or current source external forcing functions at the inputs. Use the appropriate set of specifications for each application.

switching characteristics, V_{CC} = 20 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high level output	C_L = 390 pF, R_D = 10 Ω, See Figure 1	8	16	24	ns
t_{DHL}	Delay time, high-to-low-level output		4	11	20	ns
t_{TLH}	Transition time, low-to-high-level output		8	18	30	ns
t_{THL}	Transition time, high-to-low-level output		6	16	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output		16	35	54	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	28	50	ns

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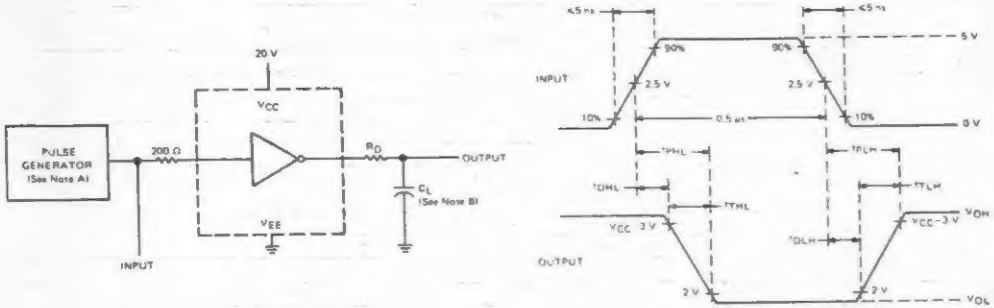
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

TOTAL DISSIPATION (BOTH DRIVERS) vs FREQUENCY

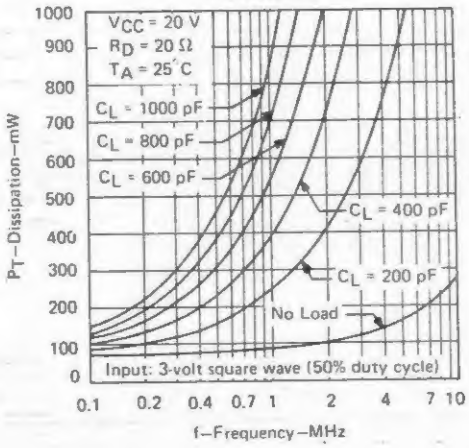


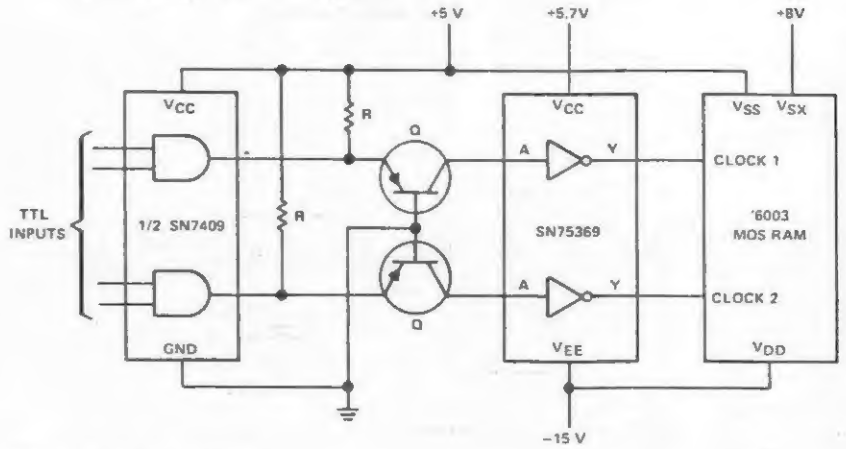
FIGURE 2

TYPICAL APPLICATION DATA

Applications of the SN75369 used as an interface device in systems converting TTL signals to negative-polarity M clock signals are shown in Figures 3 and 4. In both applications the SN75369 V_{EE} pin is connected to a negative M supply voltage. Figure 3 and 4 show the use of the SN75369 over a wide range of V_{CC} supply voltages. The device even be used as a TTL level driver, if desired, by connecting V_{CC} to 5 volts.

Both applications shown require negative level shifting from positive voltage levels to the inputs of the SN75369, w are referenced to the V_{EE} terminal. A p-n-p transistor current source is used to level shift in Figure 3. Resistor R the current and an open-collector TTL gate is used to switch the p-n-p transistor. Figure 4 shows capacitive coup being used to level shift. The SN7437 TTL buffer gate is used as a voltage source driver with pull-up resistc providing additional high-level drive. The value of coupling capacitor C depends on the frequency and characteristic the signal applied to the capacitor.

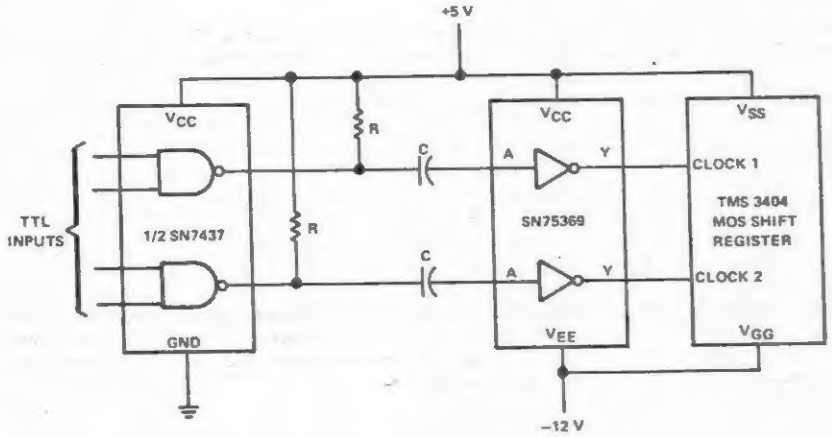
The fast switching speeds of the SN75369 may produce undersirable output transient overshoot because of loa wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient oversh The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typ value would be between 10 Ω and 30 Ω. See Figure 5.



NOTES: A. R = 350 Ω to 500 Ω.
B. Q is 2N3829 or equivalent.

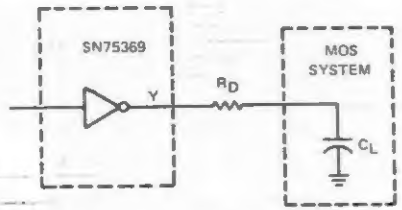
FIGURE 3–MOS RAM CLOCK DRIVER SYSTEM WITH P-N-P TRANSISTOR CURRENT SOURCE USED TO SHIFT LEVELS TO INPUTS OF SN75369

TYPICAL APPLICATION DATA



NOTE A: R = 100 Ω to 250 Ω.

FIGURE 4–MOS SHIFT REGISTER CLOCK DRIVER SYSTEM WITH CAPACITIVE COUPLING USED TO SHIFT LEVELS TO INPUTS OF SN75369



NOTE: R_D = 10 Ω to 30 Ω (optional)

FIGURE 5–USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75369 APPLICATIONS

BULLETIN NO. DL-S 7712059, SEPTEMBER 1973 — REVISED APRIL 197

DUAL READ/WRITE AMPLIFIER FOR INTERFACING BETWEEN TTL AND TMS4062-TYPE MOS RANDOM-ACCESS MEMORY (RAM)

performance features

- Node Terminals Connect Directly to I/O Terminals of TMS4062 (AMS6002) and Similar MOS RAMs
- In Write Mode, Write Driver Provides Complementary High-Voltage Outputs at Node Terminals
- In Read Mode, Read Amplifier Responds to Small Differential-Input Current in Node Terminals

ease of design features

- TTL and DTL Compatible Diode-Clamped Inputs
- TTL and DTL Compatible Data Outputs
- 50-mA Data Output Sink-Current Capability
- Data Outputs May Be Wire-AND Connected
- Operates Over Wide Range of Supply Voltages
- Minimizes or Eliminates External Components

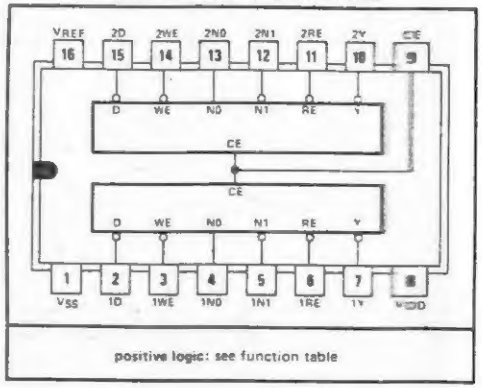
description

The SN75370 is a monolithic integrated circuit read/write amplifier that is designed to interface the Input/Output (I/O) terminals of the TMS4062 (AMS6002) and similar type MOS RAMs with TTL.

The device contains two separate channels. Each channel consists of a write driver and a read amplifier, which are common at the input/output node (N) terminals. These terminals are outputs for the write driver and inputs for the read amplifier. In the write mode, the write driver circuit is designed to write MOS-level binary information into the MOS RAM under control of TTL inputs. In the read mode, the read amplifier is designed to read MOS-level binary information from the MOS RAM and convert it to TTL levels at the data output. This is controlled by TTL inputs also.

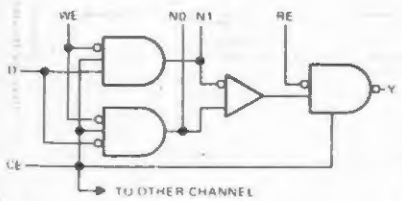
Data outputs are constructed so that they may be wire-AND connected to other outputs and/or be connected to an external pull-up resistor, if desired. The device has a chip-enable input common to both channels which can be used to enable the entire device. Internal voltage regulators permit circuit operation over a wide range of supply voltages.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see function table

functional block diagram (each channel)



FUNCTION TABLE

MODE	VOLTAGE INPUTS				VOLTAGE OUTPUTS		DIFFERENTIAL CURRENT INPUT	OUTPUT
	CE	WE	RE	D	N0	N1	N1–N0	Y
Write 0	H	L	H	L	H	L	X	H
Write 1	H	L	H	H	L	H	X	H
Read 0	H	H	L	X	L	L	L	L
Read 1	H	H	L	X	L	L	H	H
Standby	H	H	H	X	L	L	X	H
Disabled	L	X	X	X	L	L	X	Off

H = high level (voltage or current), L = low level (voltage or current), X = irrelevant
Input levels at CE, WE, RE, and D, and output levels at Y are TTL-compatible.
Voltage output levels at N fall between V_{SS} and V_{REF}.